Selective Hardening Method to Quickly Estimate the Set of Most Critical Logic Gates

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***Abstract*—It takes only eight minutes to a swirl of particles flows from the Sun to the Earth. If one of these particles hit a circuit, a fault may happens. Technology scaling makes circuits more susceptible to this radiation and brought a new challenge, design reliable circuits with the lowest cost. Selective hardening, i.e. hardening only in the most sensitive parts, is an alternative to improve reliability cost-effectively. One manner to identify the most sensitive parts of a given circuit is to define the set of more critical logic gates to the circuit reliability. Signal Probabilistic Reliability (SPR) and SPR Mult-Pass (SPR-MP) are circuit reliability estimation Methods. SPR has linear complexity but provides inaccurate results. SPR Mult-Pass (SPR-MP) is precise but has exponential time consumption. This paper compares SPR and SPR-MP, in the context of Selective Hardening, aiming to confirm SPR as a tool to identify the set of more critical logic gates. Later, we propose an optimization to quickly estimate how many gates should be hardened given an increase in the circuit reliability. The results show an improvement up to 40% when compared to previous works.**

***Index Terms*—Selective Hardening, Reliability, SPR, SPR-MP**

I. Introduction

The aggressive technology scaling has significantly affected circuits reliable operation [1]. Nanometer circuits, i.e. circuits characterized by operating in high frequencies and at a very low voltage, are more susceptible to transient faults, e.g., a single particle can trigger a failure in the circuit. Since the failure rate is increasing due to the technology scaling, circuits reliability is becoming a major factor [2].

There are several ways to estimate reliability in the literature. Three reliability estimating methods for combinational circuits, Probabilistic Transfer Matrices (PTM), Signal Probabilistic Reliability (SPR) and an SPR variation called SPR-Multipass (SPR-MP) are implemented in [3]. Among the methods, only the SPR has an inaccuracy in the presence of reconvergent fanouts. However, it is the only one scalable for current circuits.

To increase reliability, several ways of hardening a circuit are described in the literature. All these strategies and methods have some kind of penalty for the circuit, such as an increase in the area, power, and a high cost. Selective hardening emerged as a way to improve reliability cost-effectively.

In [4], the proposed strategy uses the SPR method to estimate the criticality of each logic gate. Intending to decrease the failure rate by hardening the circuit, knowing the criticality of the gates allows a better performance by the selective hardening, i.e., instead of hardening the entire circuit, hardening only the logic gates classified as critical.

This paper explores patterns between SPR and SPR-MP, aiming to confirm SPR as a method to select the set of more critical logic gates. Previous works require several runs of the SPR to estimate how many and which gates should be improved. Taking this into account, the proposed methodology, given an increase in reliability, estimates how many and which gates should be hardened, with lower time consumption.

The paper is organized as follows. Section II has three subsections, the first reviews the state-of-art in selective hardening, the second explains SPR and SPR-MP, and the third shows the metrics used to present the results. Section III contains the proposed methodology and section IV shows the results. Finally, section V contemplates the final remarks.

II. Background

This section comprises three subsections. Section A is a review of the literature in selective hardening. Section B is an overview of the methods used in the methodology while section C explains the metrics used in the results.

A. Hardening circuits

The hardening techniques aim to reduce circuits failure rate, improving their reliability. Most of these techniques work with some kind of redundancy to tolerate errors, such as error-correcting code (ECC), time redundancy with retry methods, or software to detect and recover failures [5].

When dealing with soft errors, hardware redundancy is the most effective technique but it has a high cost for the industry. Triple Modular Redundancy (TMR) is one of the most general and effective hardening techniques. It triplicates the basic system and adds voting circuits to compare the triplicated outputs and select the majority values, resulting in a large area increase [5]. With that in mind, Selective Hardening was proposed, i.e., selecting parts of the circuit to be improved rather than the entire circuit.

Create circuits with only a few more robust parts does not eliminate all the errors, but in general, the error rate is considerably reduced. It also leaves in question which parts should be hardened. The tool proposed by [2] utilizes TMR only partially to generate different versions as selective hardening to a circuit. In [6], they also work in TMR method,

seeking to improve the robustness by investigating different voter topologies.

Some methods improve reliability by working on increasing the amount of energy needed to store information. Sizing is a method that acts by increasing the necessary energy to impact the behavior of a circuit, i.e., reducing the sensitivity of the critical logic gates. A strategy that combines transistor sizing, folding, and resistors was developed by [7].

B. Circuit Reliability Estimation Methods

There are several ways to calculate circuits reliability. This subsection is intended to explain the reliability estimation methods used in the methodology.

1) Signal Probability Reliability - SPR: The SPR proposed methodology computes circuits signal reliability as a function of its logical masking capabilities, concerning multiple simultaneous faults occurrence [8]. In the method, the signal is modeled as a 2×2 matrix. This signal probability matrix represents the 4 possible states of a signal: a correct 0, a correct 1, an incorrect 0, and an incorrect 1 as shown in Figure 1.

$$P_{2\times2}(signal) = \begin{bmatrix} P(signal = correct\ 0) & P(signal = incorrect\ 1) \\ P(signal = incorrect\ 0) & P(signal = correct\ 1) \end{bmatrix}$$

Fig. 1. Matrix representation of a four-state signal probabilities [8]

The signals are modeled in the Probabilistic Transfer Matrices (PTM), well explored by [3], represents the output probability of success (q) or failure (1-q) of each input vector. The PTM matrices map all the possible inputs and their respective output's probability. Figure 2 contains a PTM matrix of a NAND logic gate.

$$\begin{array}{c} \\ \mathbf{00} \\ \mathbf{01} \\ \mathbf{10} \\ \mathbf{11} \end{array} \begin{array}{c} \begin{array}{cc} \mathbf{0} & \mathbf{1} \end{array} \\ \begin{bmatrix} 1-q & q \\ 1-q & q \\ 1-q & q \\ q & 1-q \end{bmatrix} \end{array}$$

Fig. 2. PTM matrix NAND

After defining the PTM matrix of each logic gate, the position between them is analyzed. If the logic gates are in subsequent levels it is necessary to multiply the matrices and if they are at the same level it is necessary to realize the tensor product of the matrices.

The calculation between the matrices ends when it converges to a single matrix that comprises the entire circuit. Then, the reliability is extracted from the final matrix by the summing of the correct values, correct 0 and correct 1.

SPR complexity is linear to the number of gates and this makes the method scalable to current circuits, i.e., it can be applied to circuits with thousands of logic gates. However, it has an inaccuracy in the presence of reconvergent fanouts.

2) Signal Probability Reliability Multi-Pass - SPR-MP: The SPR-Multi-Pass method is a variation of SPR that was created to deal with reconvergent fanouts. It is possible to infer from the name that the correction made is to pass the SPR multiple times. The number of times that is repass is four times for each fanout. Therefore, the cost to get the exact reliability value of this method is shown in Eq. 1.

$$SPR - MPcost = (4^f) * (SPRrun) \tag{1}$$

The cost of the SPR-MP grows exponentially with the number of fanouts. Thus, due to a large number of fanouts in current circuits, this method is impracticable.

C. Metrics

This section presents three reliability metrics [9]. The reliability (R) of a circuit is defined as the probability of a circuit operates correctly during a set interval. Therefore, its complement, the probability of a failure, it is called fault probability (P), as shown in Eq. 2.

$$P = 1 - R \tag{2}$$

One of the metrics used for reliability estimation is the failure rate (λ) calculated using Eq. 3. It indicates the number of faults that a circuit can present in a one-hour operation.

$$\lambda = -ln(R) \tag{3}$$

The Mean Time Between Failures (MTBF) that, as the name indicates, represents the time between failures in a circuit. It is an important metric used to make comparisons between the reliabilities of different systems and is calculated using Eq. 4. Once the MTBF value corresponds to the mean time between failures, as higher this value more reliable is the circuit.

$$MTBF = \frac{1}{\lambda} \tag{4}$$

III. Methodology

This section follows two main objectives. First is how to confirm the use of the SPR method as a tool in the context of selective hardening. Second is to estimate how many and which gates should be hardened, given an increase in reliability, with lower time consumption.

SPR and SPR-MP methods as mentioned in the previous section, compute the reliability based on signals, correct and incorrect. From there it is possible to simulate a hardening by increasing the success probability of a given logic gate as in the experiment described by [4].

Therefore, increasing success probability consequently increases reliability. We reproduced the proposed experiment changing the original 0.0001 failure probability to 0.00001, simulating an improved logic gate. Fig. 3 shows the original (a) and improved (b) PTM matrices for a NAND logic gate.

Then, the reliability is recalculated replacing the original matrix with the improved one. The difference between the initial reliability and the newer corresponds to the improved

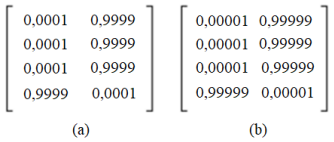

Fig. 3. PTM matrices: a) original, b) improved

gate influence in the reliability. To assess the individual influence without interference, the process is to repass the SPR for each logic gate that composes the circuit. The cost of it is equal to the number of times that the SPR runs, i.e, once for each gate improved plus the initial one, as represented by Eq. 5. Where *n* corresponds to the number of logic gates.

$$SPRcost = (n * SPRrun) + 1 \tag{5}$$

The criticality of a logic gate is given by its influence in reliability, i.e. as more influential more critical that is. Then, the information of each gate criticality is used to order them, from the most critical to the least. The same process to order gates criticality is done with the SPR-MP method aiming to check the SPR order.

A comparison between the order generated by SPR and SPR-MP can be observed in [4], showing an error rate in the positions. This difference can be justified by the fact SPR ignores reconvergent fanouts. Although this difference in the positions, it was verified that the set of most critical logic gates are almost the same. Comparisons were made between the 50% more critical logic gates to confirm the intersection between the sets.

Through the results obtained and also presented by [4], considering that a set will be select for hardening and not just a single logic gate, it is possible to confirm the use of SPR as a selective hardening tool, despite the error rate. Thus, the target is to determine how many and which gates should be hardened to achieve a given increase in the reliability using the SPR method.

Previous works, as presented by [4], consisted of improve the most critical logic gate and check if the reliability improvement has been achieved. If not, hardened the next more critical gate, until the reliability is achieved. However, this methodology requires several executions of the SPR.

Going into the next goal, the work focused on reducing the number of SPR runs to accelerate the process. We sought a way to estimate the number of logic gates that should be protected, to achieve the reliability target, but without repass the SPR exhaustively. As the requested executions for ordering the logic gates can not be reduced, the speed up will be in finding how many logic gates must be improved to achieve the goal of reliability.

In Figure 4 it is possible to visualize the reliability in terms of MTBF related to the number of improved logic gates on a scatter plot. The behavior pattern can be approximated by a power-law defined in the Eq. 6. This same behavior has been observed in other ISCAS85 benchmarks circuits [10].

$$MTBF(n) = MTBFinit.e^{cf.n} \tag{6}$$

where ***MTBFinit*** is the original circuit MTBF, *n* is the number of improved gates and *cf* is the criticality factor, obtained according Eq. 7.

$$cf = ln(MTBFfull/MTBFinit)/n \tag{7}$$

where ***MTBFfull*** corresponds to the circuit MTBF when all gates *n* are protected. From the presented model, Eq. 6 can be rewritten as Eq. 8 to provide the estimated number of logic gates that should be protected to achieve the desired MTBF.

$$n = ln(MTBFi/MTBFinit)/cf \tag{8}$$

where *n* is the estimated amount of gates that need hardening in order to increase the reliability to ***MTBFi***. Then, we can associate it with the number of gates that should be hardened without repass the SPR exhaustively. Figure 4 compares the estimation with the optimal solution in a scatter plot. Showing that the curve of our equation can overestimate and also underestimate the optimal solution.

To deal with this small difference, the proposed methodology begins with the established list of gates, protecting the previously estimated *n* more critical logic gates and run SPR. The obtained MTBF should be compared to the desired MTBF. If the value is higher, a new run should be done with one less gate. If the value is smaller, a new run should be done with one more gate. This procedure is repeated until the closer value of desired MTBF is achieved.

The proposed methodology also needs some runs of the SPR. However, as shown in the results section the number of runs is considerably reduced. The main restriction of the proposal is the use of the correct criticality order. Though, as this considers the optimal order for selective hardening, this restriction is not severe.

IV. Results

This section contains the obtained results in terms of the two main objectives. It confirms the use of the SPR method as a tool to select the set of most critical logic gates. And also quickly estimates how many and which gates should be protected given an increase in reliability.

The first objective was to demonstrate that, although the SPR method does not get the exact order, the set of most critical logic gates is similar. Whereas more than only one logic gate is selected to be hardened, the following analysis confirms SPR as a manner to identify the set of most critical logic gates rather than identify the correct order.

Table I shows the 50% more critical logic gates, ordered to the criticality, for three different circuits, C17 [10], S27 combinational version [11], and a 4-bit carry acceleration unit of a Carry Look-Ahead adder (Cla-unit). Even though SPR and SPR-MP do not generate the identical order, the gates that composes the sets are almost the same.

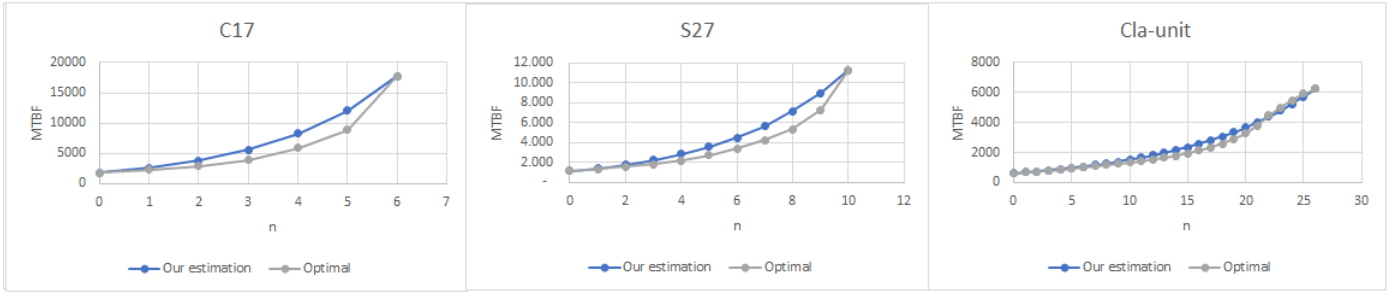

Fig. 4. MTBF optimal compared with our estimation

TABLE I
DIFFERENCE BETWEEN THE 50% MORE CRITICAL LOGIC GATES

Circuit	Method	Order	different gates
C17	SPR-MP	g3,g5,g1	-
	SPR	g1,g3,g5	
S27	SPR-MP	g7,g9,g6,g8,g0	-
	SPR	g7,g9,g6,g8,g0	
Cla-Unit	SPR-MP	g03,g10,g16,g25,g02,g24,g06, g05,g14,g23,g09,**g15,g12**	2
	SPR	g02,g03,g10,g16,g25,g06,g14, g24,g05,**g07,g04**,g09,g23	

This simplified analysis shows that the difference between the set of critical logic gates generated by each method is in the least meaningful logic gates. The obtained results and also a similar analysis in [4], motivated the remaining analysis to use the SPR to estimate the set of critical logic gates.

Thus, the proposed methodology is to use the estimation equation to extract an approximate amount of gates to be hardened, i.e., given an increase in reliability, estimate how many and which gates should be hardened.

As discussed previously, to improve the reliability of a circuit in a certain amount, previous works perform an exhaustive analysis. With our methodology, the reduction in the number of times needed to run the SPR in the circuit is presented in Table II. This analysis was extended to more ISCAS85 Bechnmarks circuits.

TABLE II
SPR RUNS TO INCREASE MTBF BY 5X

Circuit	Logic gates selecting step			Overall Reduction (Order + Select) (%)
	Proposed method	Previous works	SPR Runs Reduction(%)	
C17	1	5	80.0	36.3
S27	3	9	66.6	31.5
Cla-unit	2	20	90.0	39.1
C432	14	82	82.9	31.1
C499	3	134	97.7	40.6
C880	15	147	89.7	35.1
C1355	46	337	86.3	32.9
C1908	50	115	56.5	18.6
C2670	99	282	64.8	22.1
C3540	153	317	51.7	16.5
C5315	127	590	78.4	28.6

From the data presented in this table, it is possible to conclude that our methodology estimates how many logic gates should be protected up to 40% faster than previous ones.

V. CONCLUSIONS

Technology scaling brought the challenge of design reliable circuits with the lowest cost. Selective hardening is an alternative to improve reliability cost-effectively. One manner to identify the most sensitive parts of a circuit is to define the set of critical gates. We confirm SPR is able to identify the set of more critical logic gates. Using SPR we proposed an estimation that, given an increase in reliability, estimates how many gates should be hardened, with a lower time consumption being up to 40% faster than previous works. Future works intend to improve the proposed equation through variating cf factor.

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